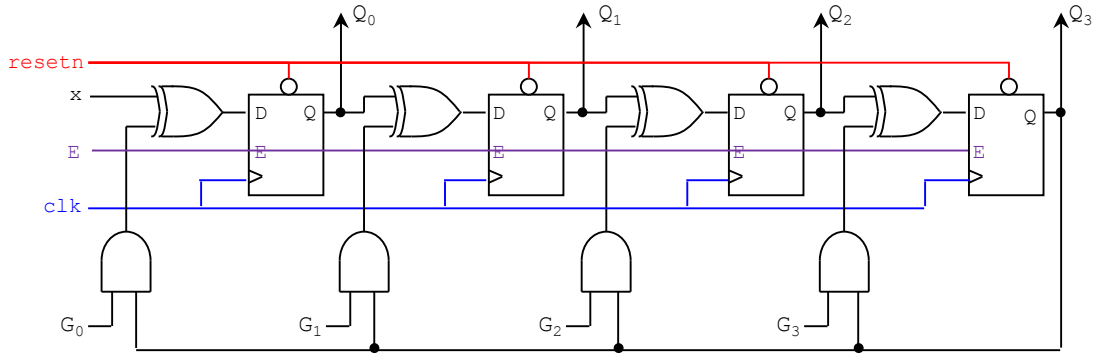
Solutions - Final Exam

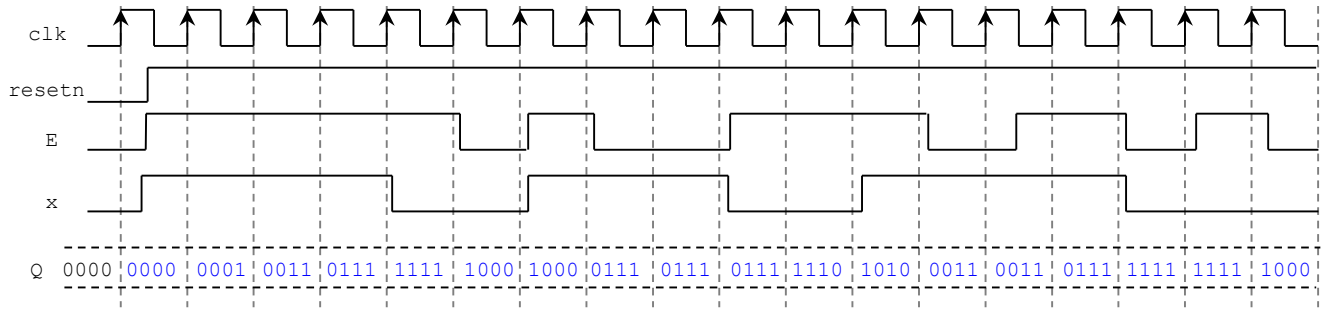
(December 14th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 PTS)

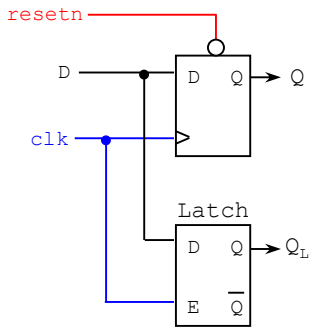
- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 0110$, $Q = Q_3Q_2Q_1Q_0$

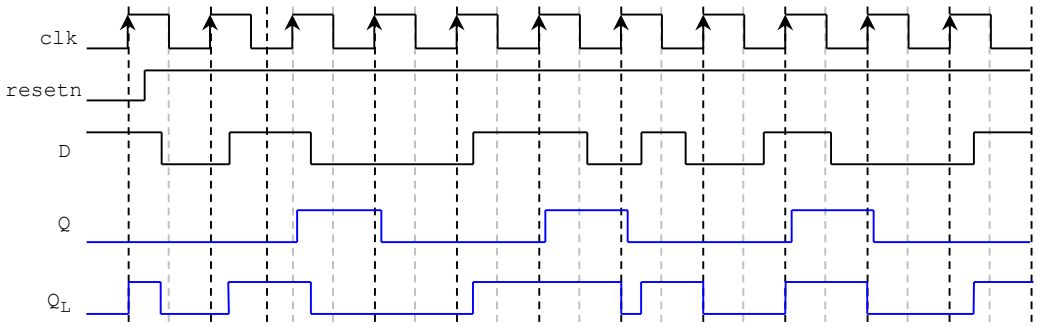




PROBLEM 2 (19 PTS)

- Complete the timing diagram of the circuit shown below: (8 pts)

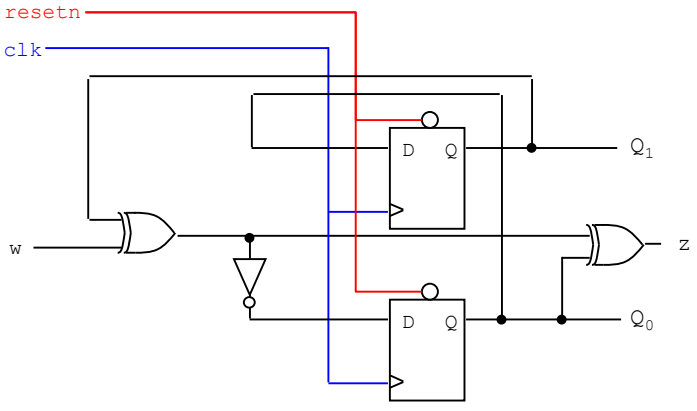




- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (11 pts)

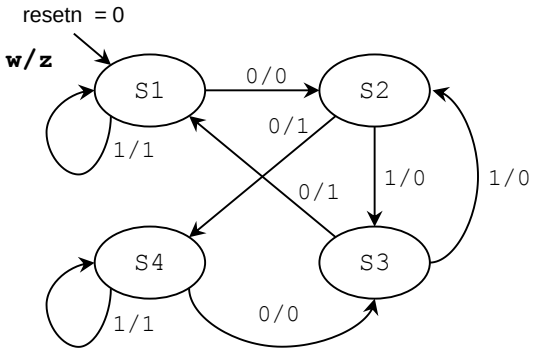
$Q_1(t+1) = Q_0(t)$
$Q_0(t+1) = \overline{Q_1(t) \oplus w}$
$z = (Q_1(t) \oplus w) \oplus Q_0(t)$

State Assignment:
S1: Q=00 S2: Q=01
S3: Q=10 S4: Q=11



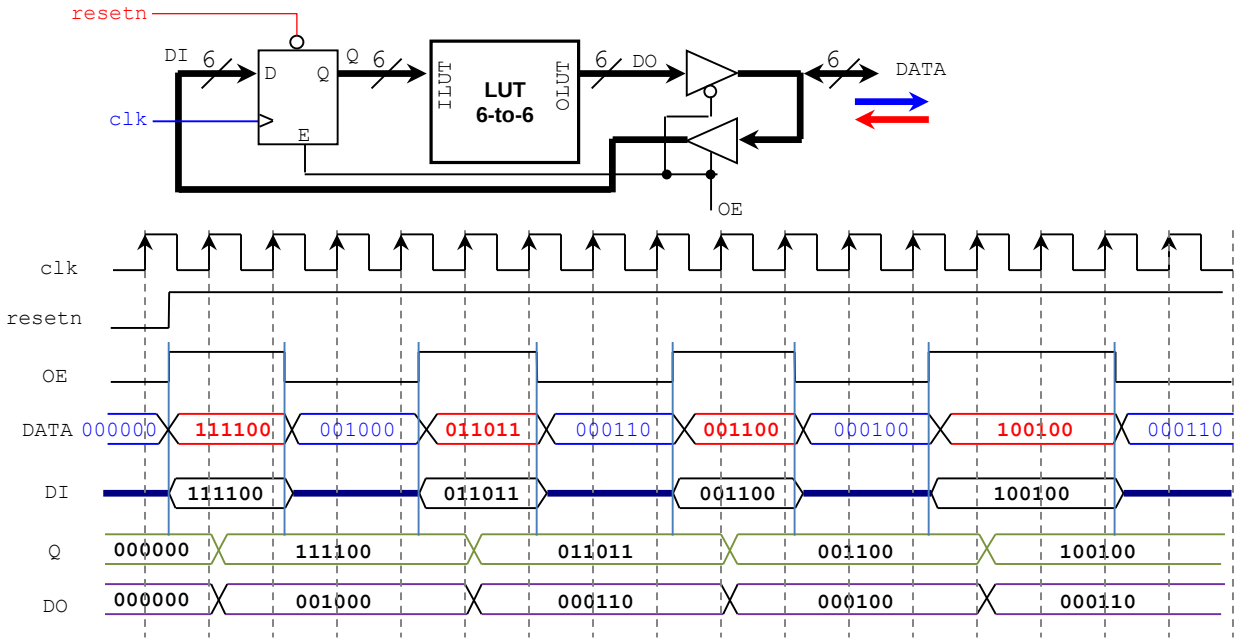
PRESENT STATE			NEXTSTATE		
w	Q_1	Q_0 (t)	Q_1	Q_0 (t+1)	z
0	0	0	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	1	1	1	1

w	PRESENT STATE	NEXT STATE	z
0	S1	S2	0
0	S2	S4	1
0	S3	S1	1
0	S4	S3	0
1	S1	S1	1
1	S2	S3	0
1	S3	S2	0
1	S4	S4	1



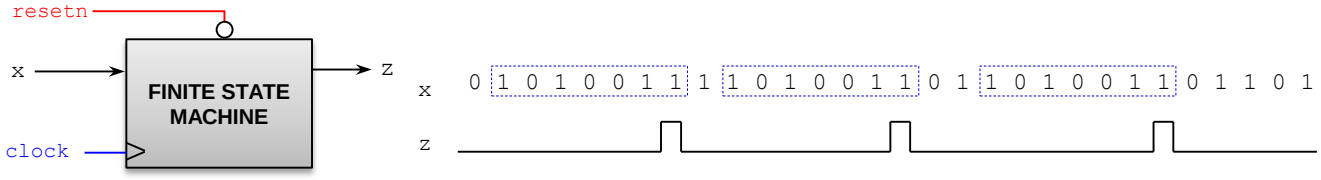
PROBLEM 3 (10 PTS)

- Given the following circuit, complete the timing diagram.
  The LUT 6-to-6 implements the following function: $OLUT = \lceil sqrt(ILUT) \rceil$, where $ILUT$ is a 6-bit unsigned number.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil sqrt(35) \rceil = 6\ (000110_2)$



PROBLEM 4 (23 PTS)

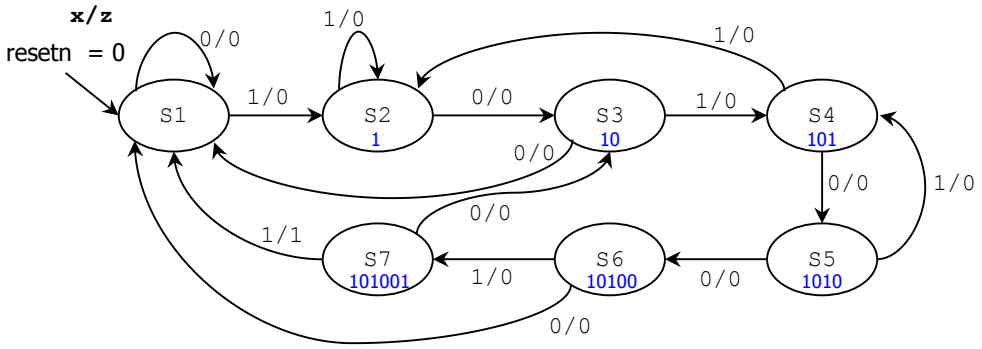
- Sequence detector: The machine has to generate $z = 1$ when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.



- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. Is this a Mealy or a Moore machine? Why? (15 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

- *State Diagram, State Table, and Excitation Table*:

  State Assignment:
  S1: Q=000 S2: Q=001 S3: Q=010
  S4: Q=011 S5: Q=100 S6: Q=101 S7: Q=110



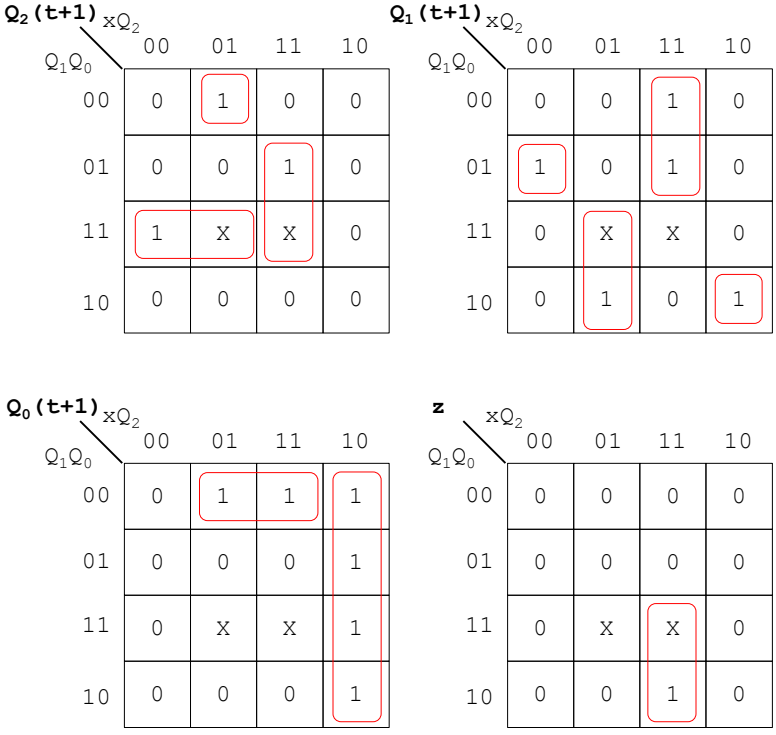
x	PRESENT STATE	NEXT STATE	z
0	S1	S1	0
0	S2	S3	0
0	S3	S1	0
0	S4	S5	0
0	S5	S6	0
0	S6	S1	0
0	S7	S3	0
1	S1	S2	0
1	S2	S2	0
1	S3	S4	0
1	S4	S2	0
1	S5	S4	0
1	S6	S7	0
1	S7	S1	1

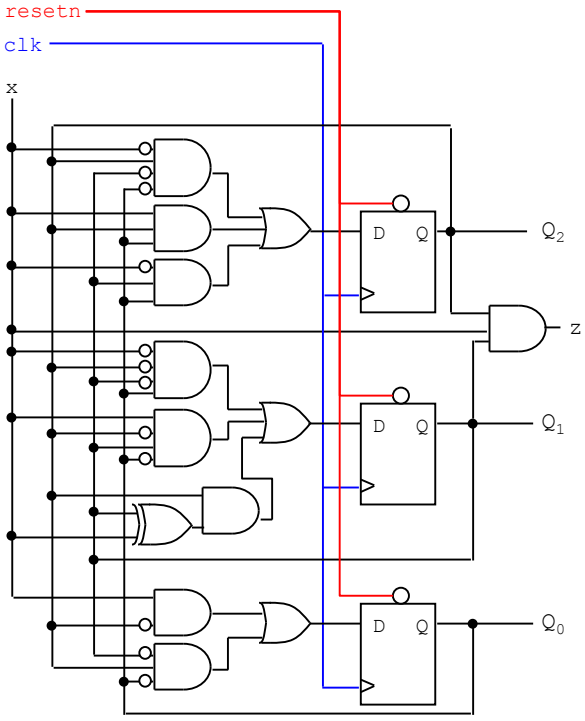
PRESENT STATE x $Q_2Q_1Q_0$(t)	NEXTSTATE $Q_2Q_1Q_0$(t+1)	z
0 0 0 0	0 0 0	0
0 0 0 1	0 1 0	0
0 0 1 0	0 0 0	0
0 0 1 1	1 0 0	0
0 1 0 0	1 0 1	0
0 1 0 1	0 0 0	0
0 1 1 0	0 1 0	0
0 1 1 1	X X X	X
1 0 0 0	0 0 1	0
1 0 0 1	0 0 1	0
1 0 1 0	0 1 1	0
1 0 1 1	0 0 1	0
1 1 0 0	0 1 1	0
1 1 0 1	1 1 0	0
1 1 1 0	0 0 0	1
1 1 1 1	X X X	X

This is a Mealy FSM. The output 'z' depends on the input as well as on the present state.

- *Excitation equations, minimization, and circuit implementation:*

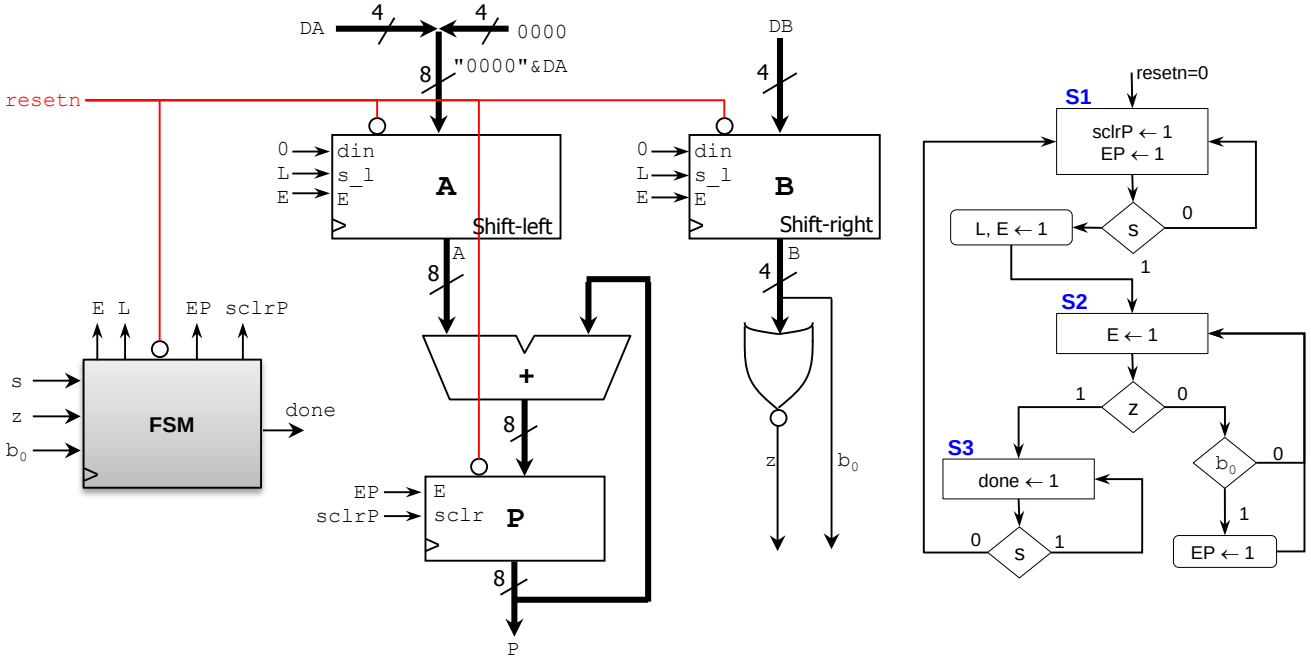
$Q_2(t+1) = \bar{x}Q_2\overline{Q_1}\,\overline{Q_0} + xQ_2Q_0 + \bar{x}Q_1Q_0$
$Q_1(t+1) = \bar{x}\overline{Q_2}\,Q_1Q_0 + x\overline{Q_2}Q_1\overline{Q_0} + xQ_2\overline{Q_1} + \bar{x}Q_2Q_1 = \bar{x}\overline{Q_2}\,\overline{Q_1}Q_0 + x\overline{Q_2}Q_1\overline{Q_0} + Q_2(x \oplus Q_1)$
$Q_0(t+1) = Q_2\overline{Q_1}\,\overline{Q_0} + x\overline{Q_2}$
$z = xQ_2Q_1$

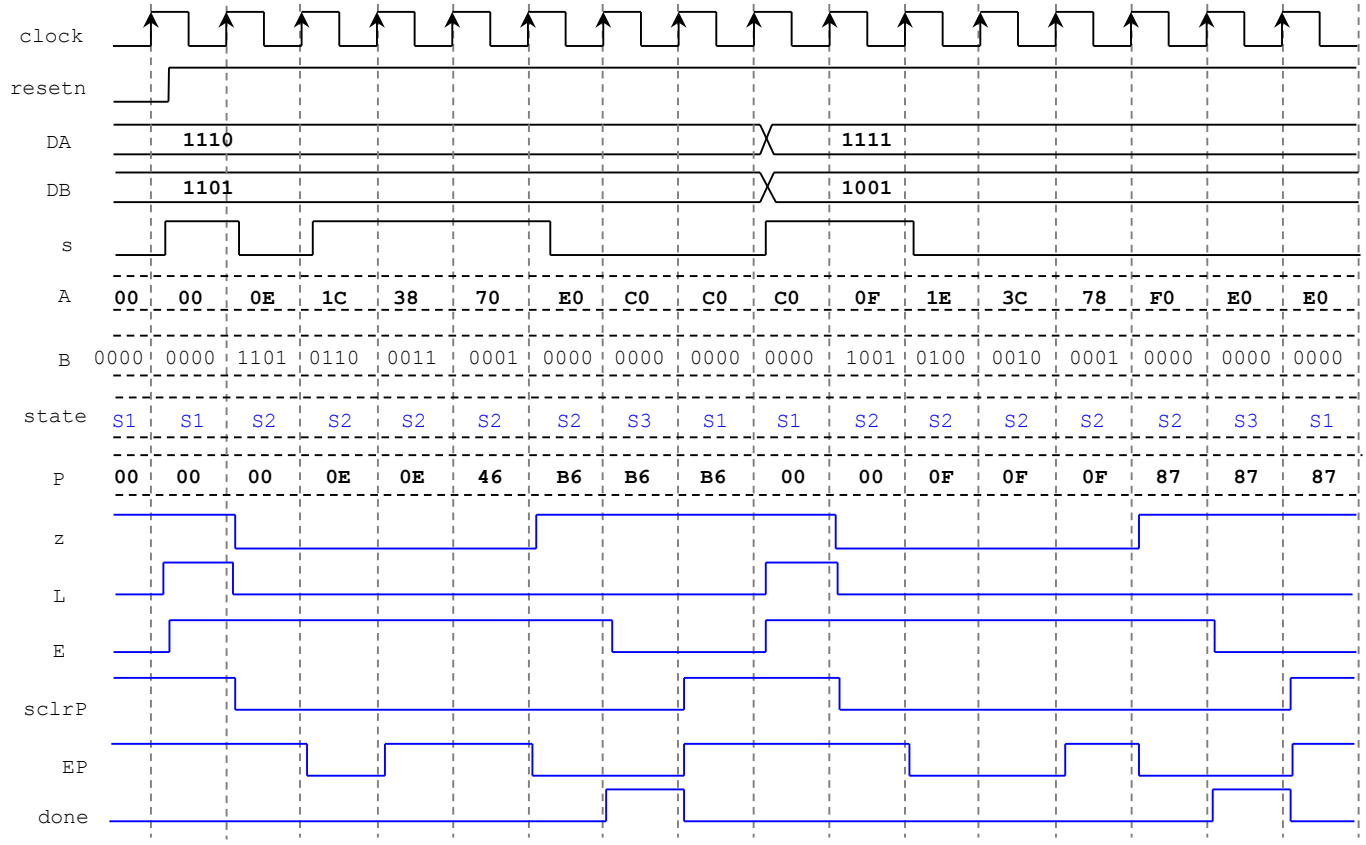




PROBLEM 5 (20 PTS)

- Complete the following timing diagram (A and P are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
  Register (for P): $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift registers (for A and B): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift



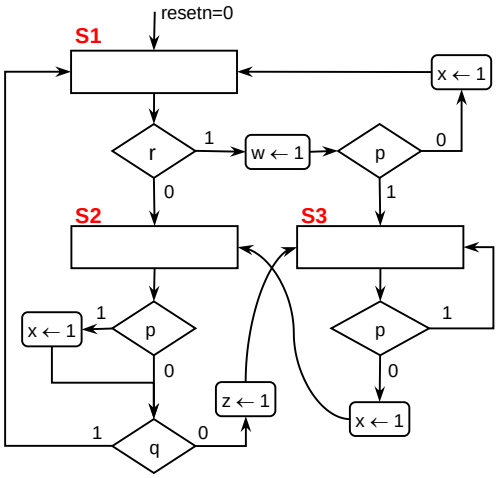


PROBLEM 6 (16 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```




```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '0' then
               y <= S2;
            else
               if p = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if q = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if p = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '1' then
                       w <= '1';
                       if p = '0' then
                          x <= '1';
                       end if;
                    end if;

         when S2 => if p = '1' then x <= '1'; end if;
                    if q = '0' then z <= '1'; end if;

         when S3 => if p = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```

This is a Mealy FSM. The outputs 'x,w,z' depend on the input as well as on the present state.